

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,960,806 B2
DATED : November 1, 2005
INVENTOR(S) : Bryant et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, Item [56] and Column 1, lines 1-3,

Title, delete "**DOUBLE GATED VERTICAL TRANSISTOR WITH DIFFERENT FIRST AND SECOND GATE MATERIALS**" and insert -- **DOUBLE GATED TRANSISTOR AND METHOD OF FABRICATION** --.

Column 11,

Line 53, delete "n-type" and insert -- p-type --.

Line 58, delete "tho" and insert -- the --.

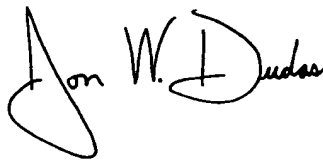
Column 12,

Line 9, delete "or claim 8" and insert -- of claim 8 --.

Line 34, delete "a first safe" and insert -- a first gate --.

Signed and Sealed this

Twenty-fourth Day of January, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office